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Sleepy keeper style based Low Power VLSI Architecture of a Viterbi Decoder applying for the Wireless LAN Operation sustainability

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Abstract
Remarkable progress in the field of wireless communication has created a research interest for Viterbi decoder with long duration of battery life, low power dissipation and portabilty in the application. Such a low power Viterbi decoder is required in the area of high speed data transfer application like communication in the convolutional coding for error free inforamtion. This article propose two strategies to enhance the execution of the decoder by circuit level design of the Viterbi decoder utilizing a sleepy keeper method with additional leakage current control transistors, which decreases the leakage power dissipation. Then at the survivor memory unit the variation is done by the usage of modified resister exchange method with search space pruning. The Simulation of the work at the semiconductor level is done with 90 nm TSMC T-SPICE and SPICE netlist is used to create the simscape application of decoder which is applied in the Matlab Communication toolbox. The outcome of the system determines that the proposed sleepy keeper Viterbi Decoder in WLAN application has a reduction of 0.24 % with QPSK and 0.13 % reduction with QAM. Also, the SNR is found to be improved at a rate of 0.5db when compared with code based Viterbi decoder.

Keywords Convolutional codes · Sleepy keeper leakage control · Power dissipation · Signal to noise ratio · T SPICE · Wireless communication · Frequency · Bit error rate

1 Introduction

Developments in the data transmission through wireless communication gets the opportunity to intrigue with different noises and disturbances. The carrier signals which convey the data bits experience [1, 2] changes in their unique substance. It brings about the degradation of the original communicated message. In order to ensure the error recovery in the information at the transmission side Convolution coder is usually utilized in the communication system. At the receiver end to get the error free signal, the maximum probability decoder that is the Viterbi decoder is outfitted to get the correct information. Yet another factor to be considered in this decoder is that the expansion in high information data transmission makes a oblige for error control coding. One of the methodologies is to utilize a error detection procedure like the Viterbi calculation, which upgrades the Bit Error Rate (BER) by means of maintaining the high information quality.

The Viterbi calculation is by all modes a productive strategy for forward Error Correction (FEC), which maintains the channel characteristics. Earlier, convolution code is commonly utilized in a few process as [3] as Physical Downlink Control Channel (PDCCH), CDMA (Code Division Multiple Access) and GSM (Global System for Mobile Communication) advanced cell, dial-up modems, satellite, profound space correspondences, and 802.11 remote LANs (Local Area Networks). The approach is found to be applied recently in Computational Linguistics, computer storage devices and Speech Recognition. Thus

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