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ORIGINAL PAPER

# FPGA Implementation of Balanced Biorthogonal Multiwavelet Using Direct Pipelined Mapping Method for Image Compression Applications

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## Abstract

An area-competent and low power pipelined direct mapping Very Large-Scale Integration Architecture for multidimensional (2D) balanced biorthogonal wavelets for image compression is discussed. The 2D architecture is realized by cascading two N points (1-D) owing to linearity, balance, and compact support of the multi-dimensionality of the biorthogonal wavelet. The discrete wavelet transforms for a 2-dimensional with balanced wavelet has been structured utilizing MATLAB program for individual modules like forwarding balanced Wavelet Transform and Inverse balanced Wavelet Transform to establish the peak signal to noise ratio (PSNR), correlation in between the recovered image and input image. The architectures are designed using Xilinx SYSgen and implemented in the Zynq 7000S devices feature a single-core ARM Cortex™-A9 processor mated with 28 nm Artix®-7 based programmable logic processor. Implementation results indicate the compression ratio is increased with less PSNR and also increases in speed with low power.

**Keywords** Wavelet Filter · Reconfigurable · Low power · Linearity · Pipeline · Logic resources · FPGA

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